The Development Board LDM-EP1C3-T100 is a printed circuit board, size 97x71x12 mm and prototypical field 71x45 mm (hole pitch 2.54 mm) with installed chip FPGA DD1 of the company Altera a family of Cyclone FPGA in the housing TQFP-100. For the convenience of the design the board under the chip DD1 is traced so that it is convenient to solder by wiring (pin in/out have appropriate areas, provided by the housing DD1, refer to pin numbers are shown in Fig. 4). The development board has a connector XS2 (IDC-10MS) to connect a download cable LDM-USB-Blaster, LDM-PB 2.01 ByteBlasterMV or its analogs (in the mode JTAG). Power can be carried out by an external source of stabilized with the voltage + 9 ... 12 V that is connected to the connector XS1. LED VD2 is a power indicator.

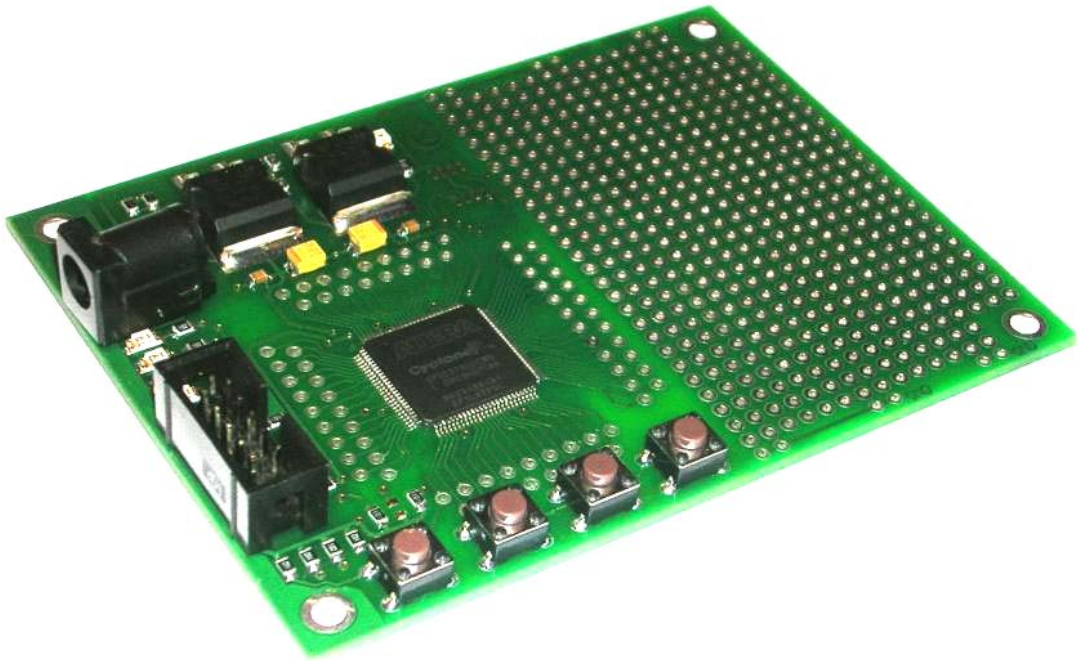

Fig. 1. General view of the development board.

Linear voltage converters DA1 and DA2 (LM317D2P) in the housing D2PAK transform supply voltage to the voltage VCCINT = 1.5 V and VCCIO = 3.3 V.

Table 1

Main characteristics of the development board.

Board Edition	Type of FPGA	Voltage FPGA, V	Number pins in/out	Logic capacity, elements LEs
LDM-EP1C3-T100	EP1C3T100	1.5	65	2 910

The board provides mounting platform for installation of chip configuration DD2 (EPCS1SI8) in the housing SOIC-8. This chip allows making configuration FPGA in the mode Active Serial. A special project – Serial FlashLoader (SFL) – is downloaded for programming configurative ROM in FPGA on JTAG-interface. SFL is a bridge between interfaces JTAG and Active Serial that transforms data receiving from JTAG-interface to the required format for programming consistent configuration ROM.

The development board is intended for prototyping devices designed on FPGA of the company Altera a family of ACEX 1K, and also for assembly completed devices by mounting necessary components on the prototypical field of the board. Use of LDM-EP1C3-T100 allows minimizing the implementation time of the product on the market.

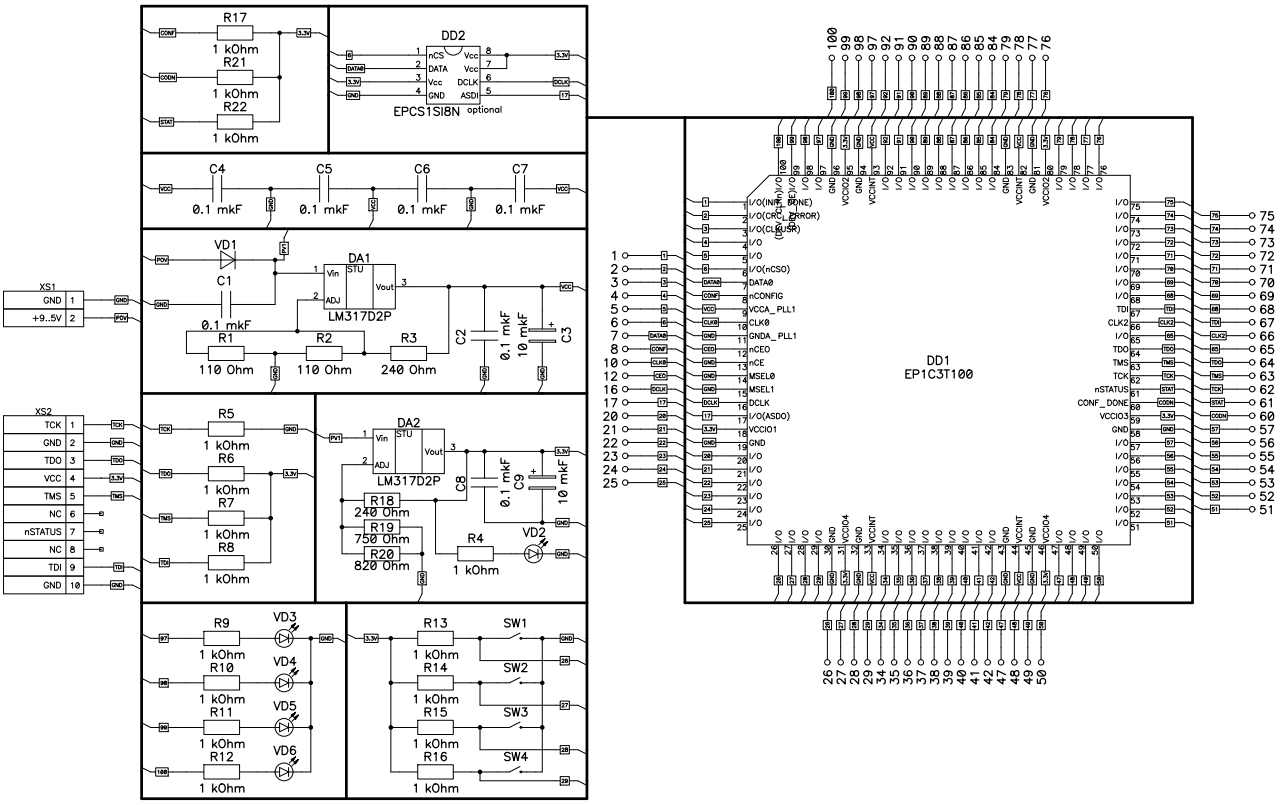

Fig. 2. The electrical scheme.

There are four LEDs VD3-VD6 and four buttons SW1-SW4 on the board which are connected with FPGA. It is intended for simplification of designing and can be useful during the test of project.

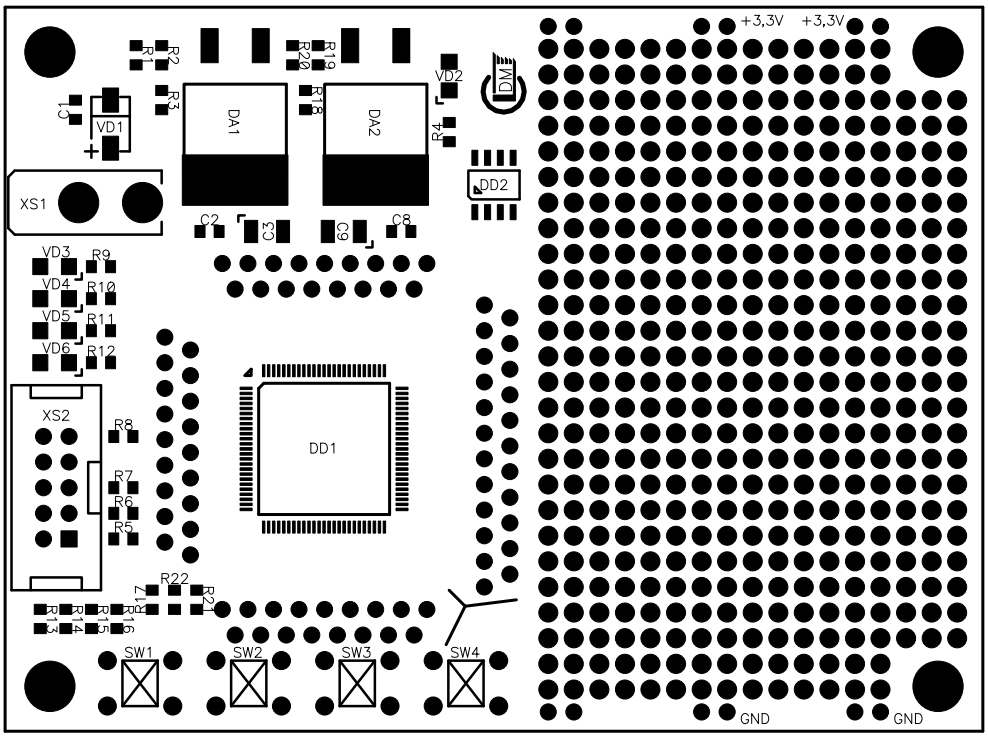

Fig. 3. External view of the printing board.

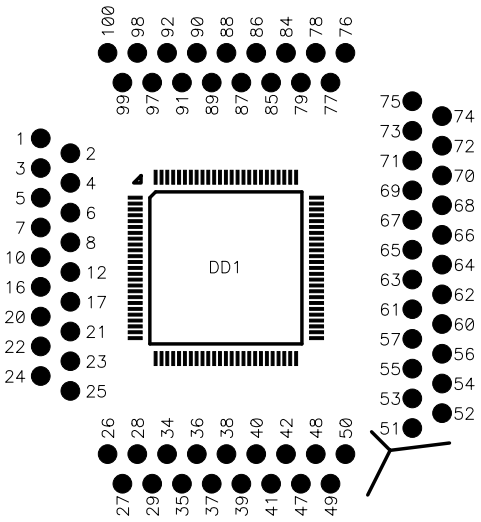

Fig. 4. Designation of mounting pads.

Packaging arrangements:

- The development board;
- Description of the development board;
- Examples of projects for Quartus II Web Edition Software;
- Description of the family of FPGA Altera.