The download cable LDM-PB 2.01 ByteBlasterMV is connected to LPT port of a personal computer and allows:

- to carry out configuration a family of FPGA Altera, making in accordance with the technology of SRAM: Stratix® II, Stratix GX, Stratix, Cyclone™ III, Cyclone™ II, Cyclone, APEX™ II, APEX 20K (including APEX 20K, APEX 20KE, and APEX 20KC), ACEX® 1K, Mercury™ , FLEX® 10K (including FLEX 10KA and FLEX 10KE), FLEX 8000, FLEX 6000 and Excalibur™.
- to provide with programming a family of CPLD Altera, making in accordance with the technology of EEPROM: MAX® II, MAX 9000, MAX 7000S, MAX 7000AE, MAX 7000B и MAX 3000A.
- to produce programming of configurative PROM: EPC2, EPC4, EPC8 and EPC16.

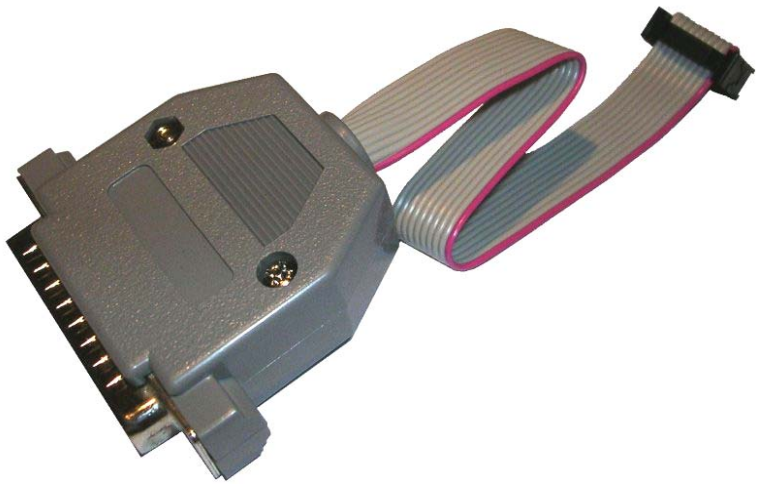

Fig. 1. General view of the download cable LDM-PB 2.01 ByteBlasterMV

Special features of the download cable:

- allows programming chips that are powered of 5.0 V or 3.3 V;
- carries out the way of quick and cheap intersystem programming;
- supports downloading data directly from the design environment MAX+PLUS II and Quartus II;
- compatible with the standard 25-contacts parallel port (LPT) of a personal computer;
- has a standard user 10-contact connector to connect to the board.

Download modes

ByteBlasterMV has two download modes (Table 1).

Table 1

Modes of cable download LDM-PB 2.01 ByteBlasterMV

Passive consecutive mode PS	– is used for the chip configuration: APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000 and ACEX 1K
Mode JTAG	– industrial standard interface for the chip programming: APEX 20K, FLEX 10K, MAX 9000, MAX 7000S, MAX 7000A, MAX 3000A, MAX® II, Cyclone™ III, Cyclone™ II, Cyclone, ACEX 1K, EPC2, EPC4, EPC8 and EPC16

Correspondence interface cable signals and parallel port contacts refer to the Table 2. The scheme of the download cable LDM-PB 2.01 ByteBlasterMV refers to the Fig. 2.

Table 2

Correspondence interface cable signals and parallel port contacts

Contact	PS Mode	JTAG Mode
2	DCLK	TCK
3	nCONFIG	TMS
8	DATA0	TDI
11	CONF_DONE	TDO
13	nSTATUS	-
15	VCC	VCC
18-25	GND	GND

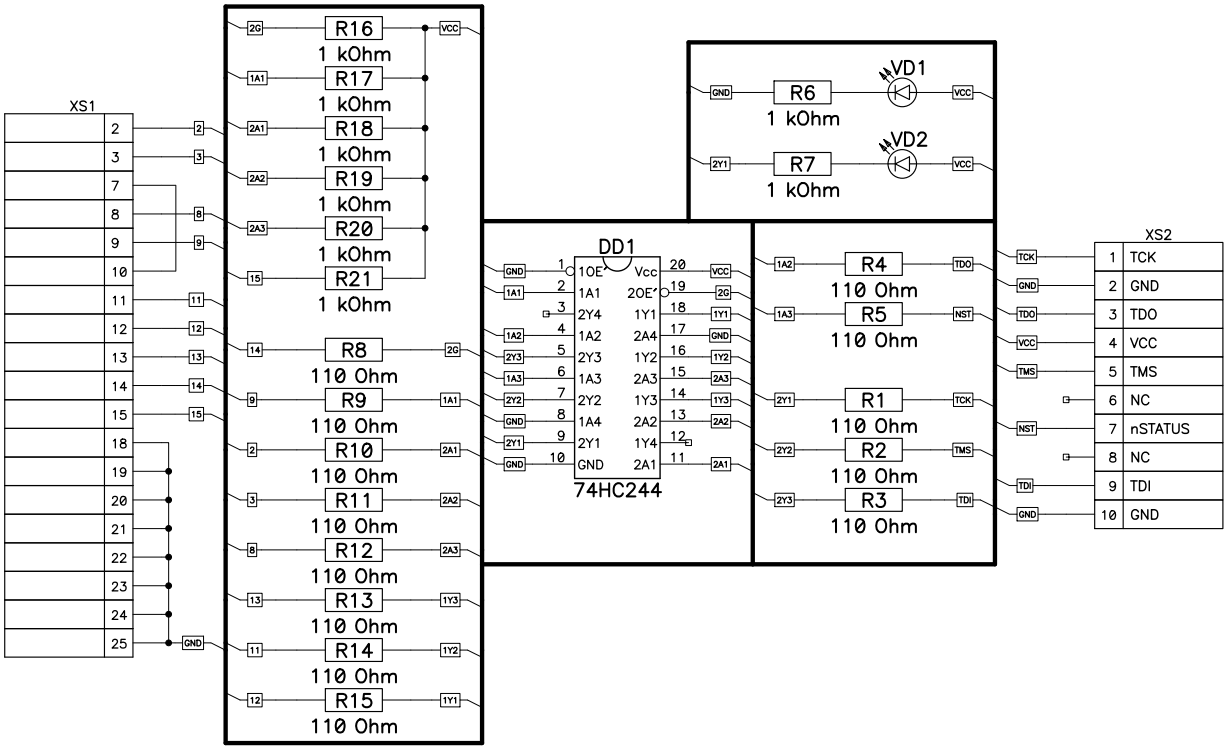

Fig. 2. The scheme LDM-PB 2.01 ByteBlasterMV

10-contact connector is shown in the Fig. 3, allocation of its contacts is shown in the Table 3.

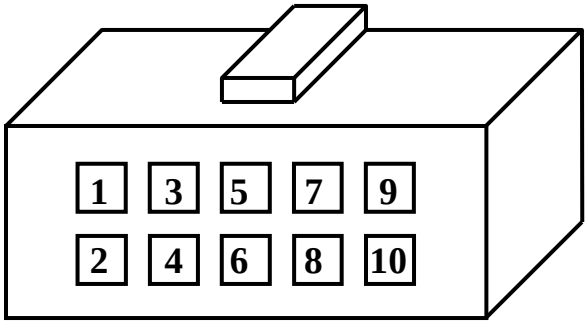

Fig. 3. The view of 10-contact connector LDM-PB 2.01 ByteBlasterMV

Table 3

Outputs designation of the 10-contact connector LDM-PB 2.01 ByteBlasterMV

Contact	PS-mode		JTAG-mode	
	Designation	Description	Designation	Description
1	DCLK	Clock signal	TCK	Clock signal
2	GND	Earth	GND	Earth
3	CONF_DONE	Configuration status control	TDO	Data output
4	VCC	Supply voltage	VCC	Supply voltage
5	nCONFIG	Configuration status control	TMS	Direction of the final automatic machine JTAG
6	-	Does not use	-	Does not use
7	nSTATUS	Configuration status	-	Does not use
8	-	Does not use	-	Does not use
9	DATA0	Data input	TDI	Data input
10	GND	Earth	GND	Earth

Power of LDM-PB 2.01 ByteBlasterMV is carried out by the board, on which a program device is installed. During the use of development boards or sockets for programming, it is imperative to set power blocking capacitors. The absence of such capacitors may cause problems in programming and even damage the chip.

Supply voltage range:

- 4.5 - 5.5 for devices with VCC=5 V;
- 2.5 - 3.6 for devices with VCC=3 V.

Packaging arrangements:

- The download cable LDM-PB 2.01 ByteBlasterMV;
- Description of the download cable;
- Examples of projects for Quartus II Web Edition Software;
- Description of the family of FPGA Altera.