The seria of development boards XB-XC3Sxxx-PQ208 is a printed circuit board, size 145x122x12 mm and prototypical field 70x122 mm (hole pitch 2.54 mm) with installed chip FPGA DD1 of the company Xilinx a family of Spartan-3 FPGA in the housing PQFP-208. For the convenience of the design the board under the chip DD1 is traced so that it is convenient to solder by wiring (pins in/out have appropriate areas, provided by the housing DD1). The development board has a connector XS2 (IDC-10MS) to connect download cables XB-XUP USB-JTAG, XB-PCIII 2.01 Xilinx Parallel Cable III or its analogs. The power is carried out by an external stabilized source with the voltage + 9...12 V, that is connected to the connector XS1. LED VD2 is a power indicator.

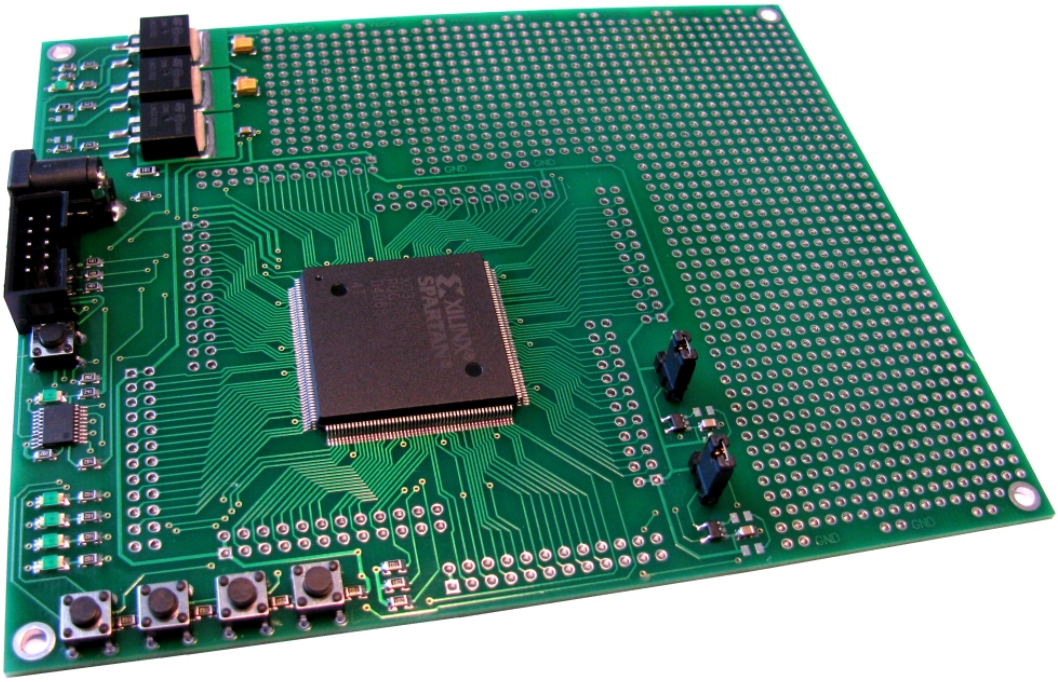


Fig. 1. General view of the development board.

Linear voltage converters DA1, DA2 and DA3 (LM317D2P) in the housing D2PAK transform supply voltage into a voltage VCCINT = 1.2 B, VCCAUX = 2.5 V and VCCIO = 3.3 V.

Table 1

Main characteristics of the development board

Type of the board	Type of FPGA	Supply voltage FPGA VCCINT, V	Number of pins in/out	Logical capacity, logical cell
XB-XC3S50-PQ208	XC3S50-PQ208	1.2	124	50 000
XB-XC3S200-PQ208	XC3S200-PQ208	1.2	141	200 000
XB-XC3S400-PQ208	XC3S400-PQ208	1.2	141	400 000

The development board is intended for prototyping devices designed on FPGA of the company Xilinx a family of Spartan-3 FPGA, and also for assembly completed devices by mounting necessary components on the prototypical field of the board. Use of XB-XC3Sxxx-PQ208 allows minimizing the implementation time of the product on the market.

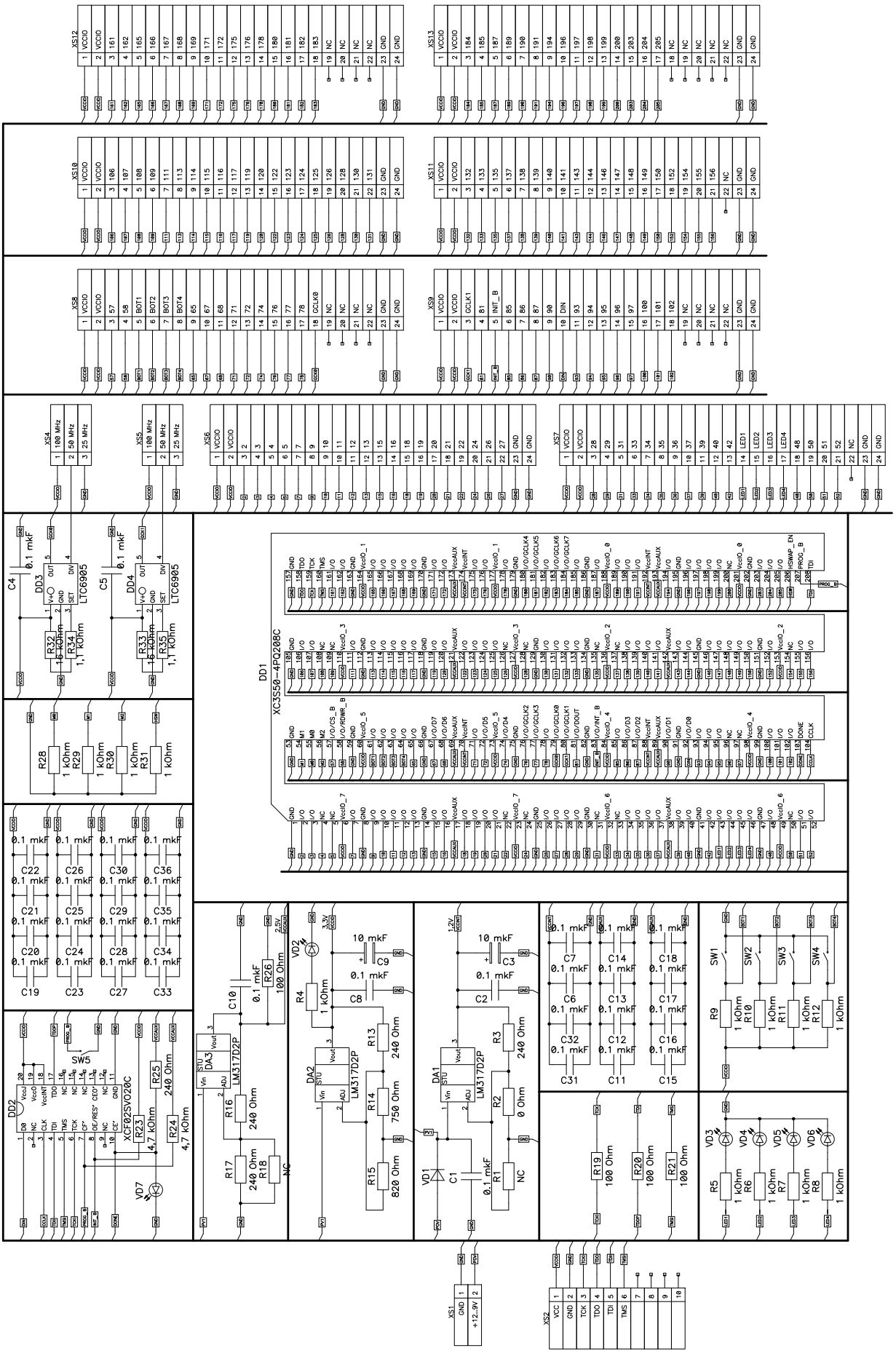


Fig. 2. The electrical scheme XB-XC3S50-PQ208

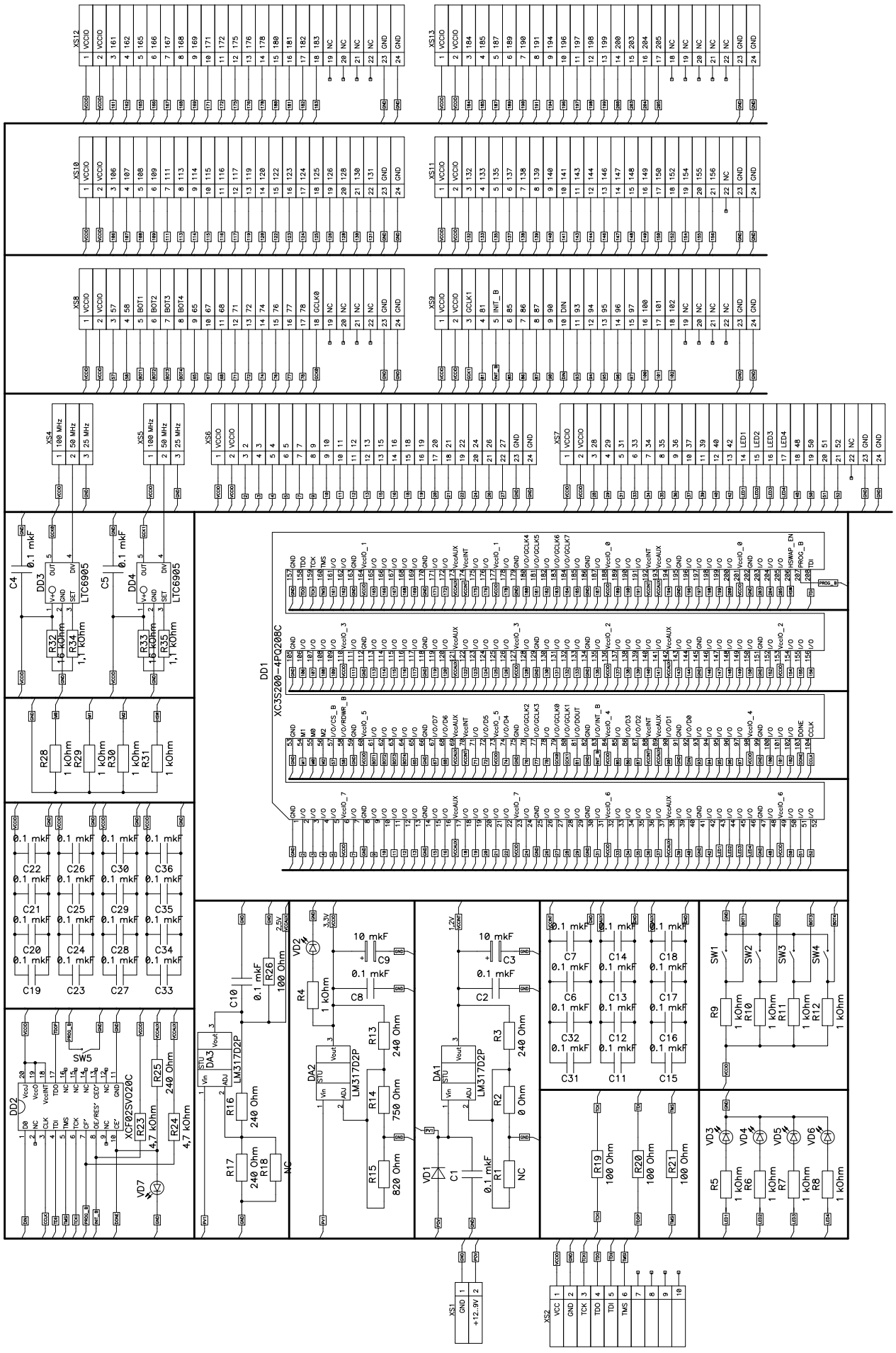


Fig. 3. The electrical scheme XB- XC3S200-PQ208

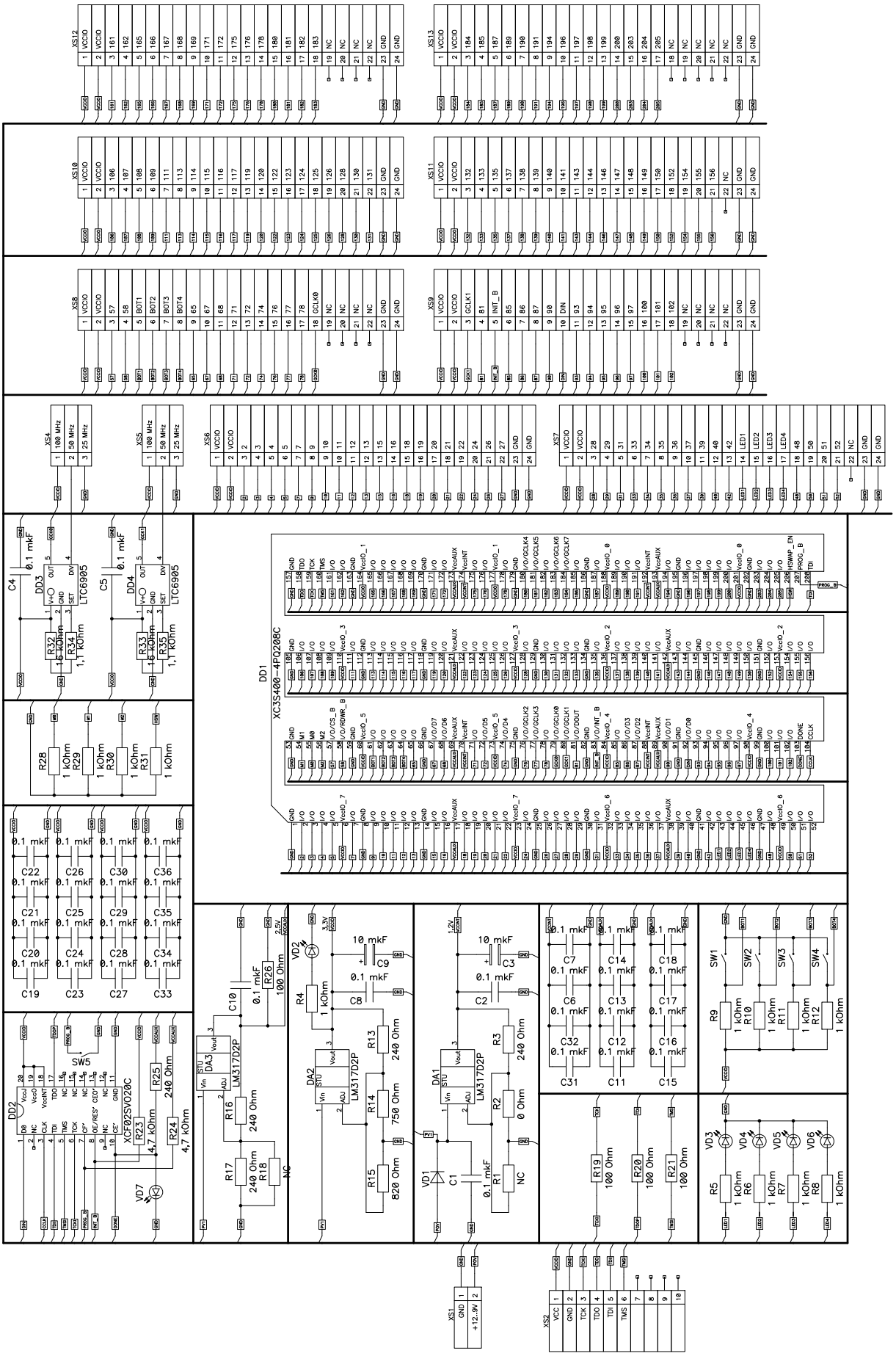


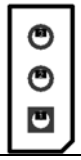
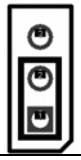
Fig. 4. The electrical scheme XB- XC3S400-PQ208

There are four LEDs VD3-VD6 and four buttons SW1-SW4 on the board which are connected with FPGA. It is intended for simplification of designing and can be useful during the test of project.

The board has two separate generators DD3 and DD4. Using jumpers XS4 and XS5, you can set generators for the frequency 25, 50 and 100 MHz (Table 2).

Table 2

Setting generators for the frequency

25 MHz	50 MHz	100 MHz
		

The board has configurative memory PROM XCF02SVO20C (DD2) with memory capacity 2 Mbit. Memory programming is carried out by connector XS2. For successful programming of configuration memory and FPGA it is necessary to set properly programming mode of the board in the system Xilinx ISE WebPack. For this, set the order of placing the FPGA and PROM, as shown in Figure 5. The first line TDI is the FPGA, followed by the PROM.

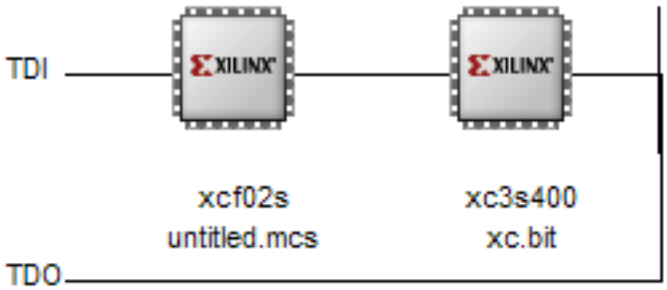


Fig. 5. the order placing the FPGA and PROM in the system Xilinx ISE WebPack

The LED VD7 is an indicator of programming the configuration PROM. Button SW5 is to restart the process of configuring the FPGA configuration by the code from the configuration PROM.

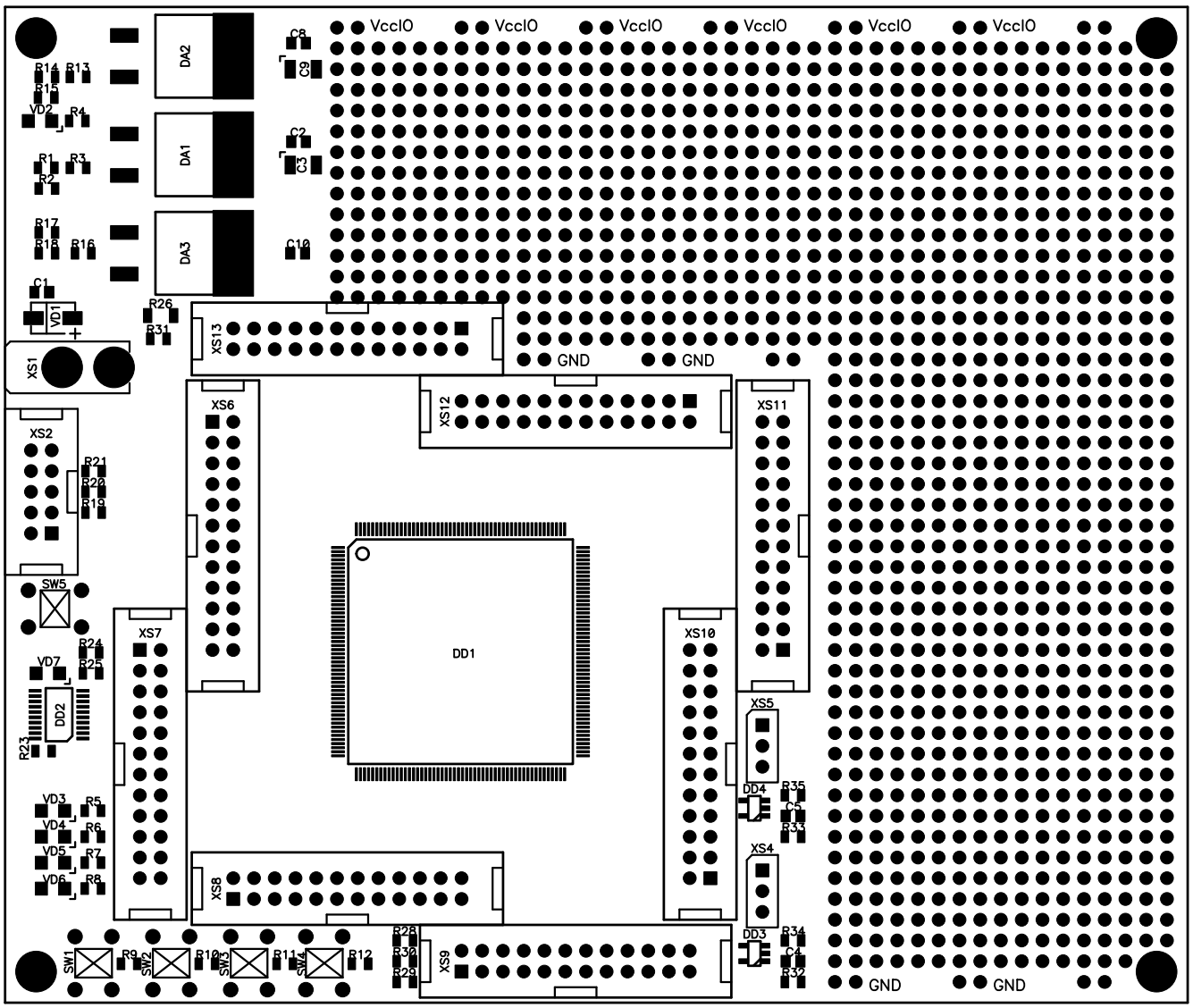


Fig. 6. External view of the printing board.

Packaging arrangements:

- The development board;
- Description of the development board;
- Examples of projects for Xilinx ISE WebPack;
- Description of the family of FPGA Xilinx.