The seria of development boards XB-XC95xxxXL-TQ144 is a printed circuit board, size 133x102x12 mm and prototypical field 58x102 mm (hole pitch 2.54 mm) with installed chip FPGA DD1 of the company Xilinx a family of XC9500XL CPLD in the housing TQFP-144. For the convenience of the design the board under the chip DD1 is traced so that it is convenient to solder by wiring (pins in/out have appropriate areas, provided by the housing DD1). The development board has a connector XS2 (IDC-10MS) to connect download cables XB-XUP USB-JTAG, XB-PCIII 2.01 Xilinx Parallel Cable III or its analogs. The power is carried out by an external stabilized source with the voltage + 9...12 V, that is connected to the connector XS1. LED VD2 is a power indicator.

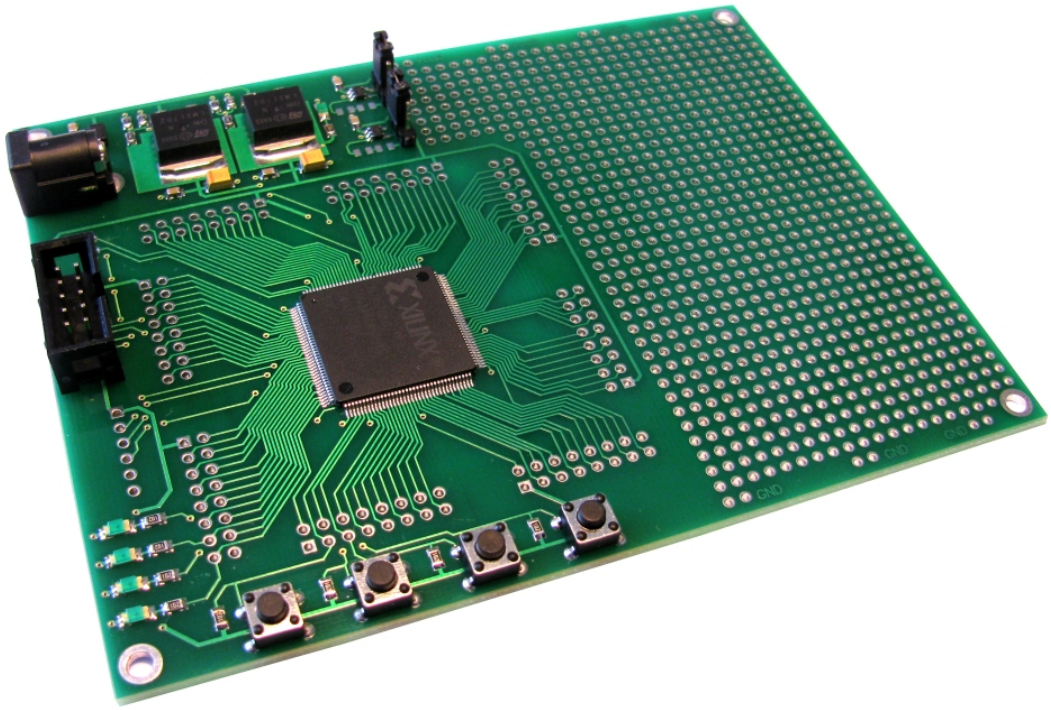


Fig. 1. General view of the development board.

Linear voltage converters DA1 and DA2 (LM317D2P) in the housing D2PAK transform supply voltage into a voltage VCCINT = 3.3 V and VCCIO = 3.3 V.

Table 1

Main characteristics of the development board

Type of the board	Type of FPGA	Supply voltage FPGA VCCINT, V	Number of pins in/out	Logical capacity, valves
XB-XC95144XL-TQ144	XC95144XL-TQ144	3.3	117	3 200
XB-XC95288XL-TQ144	XC95288XL-TQ144	3.3	117	6 400

The development board is intended for prototyping devices designed on FPGA of the company Xilinx a family of XC9500XL CPLD, and also for assembly completed devices by mounting necessary components on the prototypical field of the board. Use of XB-XC95xxxXL-TQ144 allows minimizing the implementation time of the product on the market.

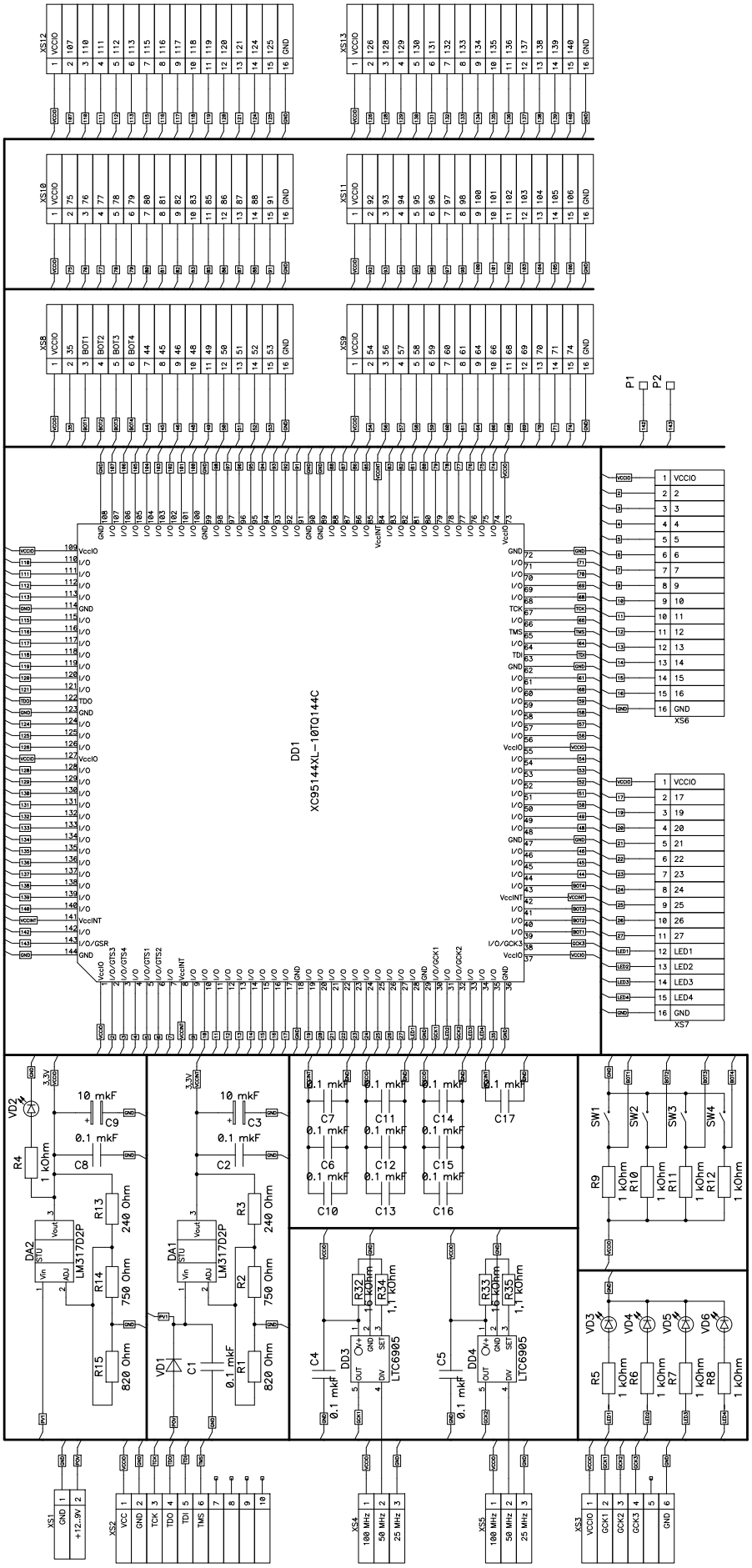


Fig. 2. The electrical scheme XB-XC95144XL-TQ144

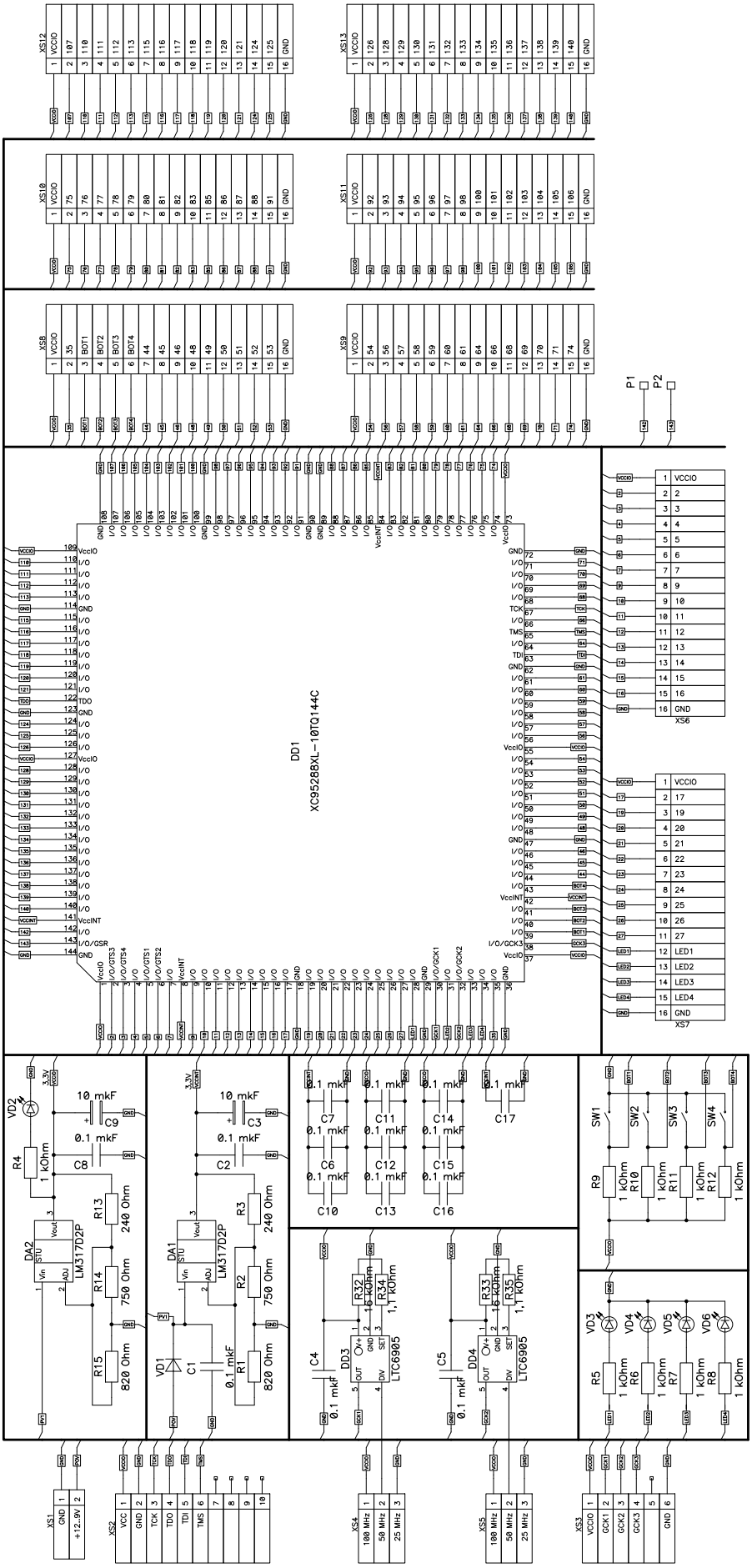


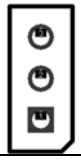
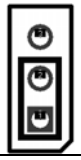
Fig. 3. The electrical scheme XB-XC95288XL-TQ144

There are four LEDs VD3-VD6 and four buttons SW1-SW4 on the board which are connected with FPGA. It is intended for simplification of designing and can be useful during the test of project.

The board has two separate generators DD3 and DD4. Using jumpers XS4 and XS5, you can set generators for the frequency 25, 50 and 100 MHz (Table 2).

Table 2

Setting generators for the frequency

25 MHz	50 MHz	100 MHz
		

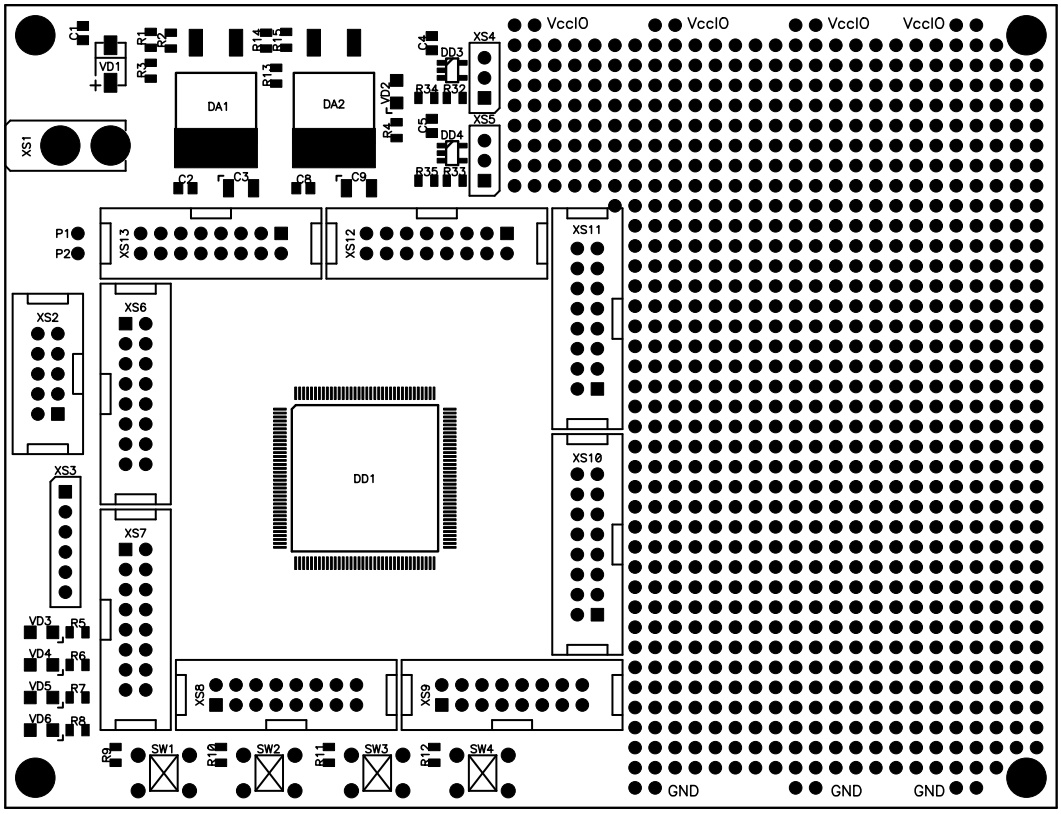


Fig. 4. External view of the printing board.

Packaging arrangements:

- The development board;
- Description of the development board;
- Examples of projects for Xilinx ISE WebPack;
- Description of the family of FPGA Xilinx.